Remarks

Please enter and consider new claims 40-49. Support for new claims 40-44 may be found, e.g., in the Specification at page 5, line 27 through page 11, line 11. Support for claims 45-49 may be found, e.g., in the Specification at page 5, line 27 through page 11, line 11, and page 14, lines 15-24.

Species Election

Applicant submits that new claims 40-49 are readable on the species that the Examiner indicated is illustrated in Figure 1. Applicant elected such species in the Response to Restriction Requirement dated 3 June 2002. As a result of this Preliminary Amendment, Applicant submits that claims 23-26, 37-49 are readable on the elected species.

Conclusion

The Examiner is invited to contact Applicant's Representatives, at the below-listed telephone number, if there are any questions regarding this Preliminary Amendment or if prosecution of this application may be assisted thereby.

CERTIFICATE UNDER 37 C.F.R. § 1.8:

The undersigned hereby certifies that this paper is being transmitted by facsimile in accordance with 37 C.F.R. § 1.6(d) to the Patent and Trademark Office, addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on this 7 day of June, 2002, at 12:08 (Central Time).

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7 June 2002
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APPENDIX A - PENDING CLAIMS
Serial No.: 09/942,200
Docket No.: 150.00640102

23. A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a barrier layer over at least a portion of the surface, wherein the barrier layer is formed of a platinum(x):ruthenium(1-x) alloy, where x is in the range of about 0.60 to about 0.995.

24. The structure of claim 23, wherein x is in the range of about 0.90 to about 0.98.

25. The structure of claim 24, wherein x is about 0.95.

26. The structure of claim 23, wherein the portion of the surface is a silicon containing surface.

27. A capacitor structure comprising:

a first electrode;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a barrier layer of platinum(x):ruthenium(1-x) alloy.

28. The structure of claim 27, wherein x is in the range of about 0.60 to about 0.995.

29. The structure of claim 28, wherein x is in the range of about 0.90 to about 0.98.

30. The structure of claim 27, wherein at least one of the first electrode and second electrode comprises the barrier layer of platinum(x):ruthenium(1-x) alloy and one or more additional conductive layers.

31. The structure of claim 30, wherein the one or more additional conductive layers are formed from materials selected from materials selected from the group of metals and metal alloys; metal and metal alloy oxides; metal nitrides; and metal silicides.

32. A memory cell structure comprising:

a substrate assembly including at least one active device; and

a capacitor formed relative to the at least one active device, the capacitor comprising at least one electrode including a barrier layer formed of platinum(x):ruthenium(1-x) alloy.

33. The structure of claim 32, wherein the capacitor includes:

a first electrode formed relative to a silicon containing region of the at least one active device;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein the first electrode comprises the barrier layer formed of platinum(x):ruthenium(1-x) alloy.

34. The structure of claim 33, wherein the first electrode comprising the barrier layer formed of platinum(x):ruthenium(1-x) alloy includes one or more additional conductive layers.

35. The structure of claim 33, wherein x is in the range of about 0.60 to about 0.995.

36. The structure of claim 35, wherein x is in the range of about 0.90 to about 0.98.

37. An integrated circuit structure comprising:

a substrate assembly including at least one active device; and

an interconnect formed relative to the at least one active device, the interconnect including a barrier layer formed of platinum(x):ruthenium(1-x) alloy.

38. The structure of claim 37, wherein x is in the range of about 0.60 to about 0.995.

39. The structure of claim 38, wherein x is in the range of about 0.90 to about 0.98.

40. **(New)** The structure of claim 23, wherein the barrier layer comprises a chemical vapor deposited barrier layer.

41. **(New)** The structure of claim 23, wherein the at least a portion of the surface defines a small high aspect ratio opening.

42. **(New)** The structure of claim 23, wherein a thickness of the barrier layer is in a range of about 10 Å to about 10,000 Å.

43. **(New)** The structure of claim 42, wherein the thickness of the barrier layer is in a range of about 100 Å to about 500 Å.

44. **(New)** The structure of claim 23, wherein the substrate assembly comprises at least one active device.

45. **(New)** The structure of claim 37, wherein the barrier layer comprises a chemical vapor deposited barrier layer.

46. **(New)** The structure of claim 37, wherein the substrate assembly comprises a small high aspect ratio opening, and further wherein the interconnect is formed in the small high aspect ratio opening relative to the at least one active device.

47. **(New)** The structure of claim 37, wherein a thickness of the barrier layer is in a range of about 10 Å to about 10,000 Å.

48. **(New)** The structure of claim 47, wherein the thickness of the barrier layer is in a range of about 100 Å to about 500 Å.

49. **(New)** The structure of claim 39, wherein x is about 0.95.